CLAIM AMENDMENTS

1. (currently amended) An on-chip inductor consisting of:

a first dielectric layer;

a conductive winding on the first dielectric layer;

a second dielectric layer having a major surface parallel to a major surface of the first dielectric layer;

a P-well having a major surface parallel to [[a]] the major surface of the first dielectric layer; and

a substrate having a major surface parallel to the major surface of the first dielectric layer.

2. (currently amended) ~~The on-chip inductor of claim 1 further consists of~~ An on-chip inductor consisting of:

a first dielectric layer;

a conductive winding on the first dielectric layer;

a second dielectric layer having a major surface parallel to a major surface of the first dielectric layer;

a P-well having a major surface parallel to [[a]] the major surface of the first dielectric layer;

a field oxide having a major surface that is juxtaposed to the major surface of the P-well; and

a substrate having a major surface parallel to the major surface of the first dielectric layer.

3. (previously presented) The on-chip inductor of claim 1 wherein:

the conductive winding is a spiral winding.

4 - 8. (canceled).

9. (currently amended) An on-chip inductor consisting of:

a first dielectric layer;

a conductive winding on the ~~at least one~~ first dielectric layer;

a second dielectric layer having a major surface parallel to a major surface of the first dielectric layer;

a field oxide layer having a major surface parallel to [[a]] the major surface of the first dielectric layer; and

a substrate having a major surface parallel to the major surface of the first dielectric layer.

10 -30. (canceled)